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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,209	04/21/2004	Dwadasi Hare Rama Sarma	DP-305691	3208

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,209	SARMA ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5 and 11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to amendment filed on April 4, 2006.

Election/Restrictions

2. Applicant's traversal of restriction requirement on the ground that the search for both groups together will not be burdensome to the examiner is not found persuasive. As explained in the previous action invention of both the group are distinct and are classified in different classes a thorough search of both the groups and all the species will need more time and will be burdensome to the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polinski (US Patent No. 5,386,339).

Regarding claim 1, Polinski, in an embodiment of figure 5, discloses a circuit board assembly comprising: a co-fired substrate comprising at least first (made up of sheet 122) and second (made up of 148) regions superimposed and bonded to each other, the first region being formed of a plurality of first ceramic layers (LTCC sheet 122), each first ceramic layer consisting essentially of electrically-nonconductive materials (dielectric structure 124, column 6, line 1,2), at least some of the first ceramic layers being bonded to each other (see figure), the second region being formed of at least one second ceramic layer (148), conductor lines on at least some of the first ceramic layers so as to be between adjacent pairs of the first ceramic layers; electrically-conductive vias that extend through at least some of the first ceramic layers and electrically interconnect the conductor lines on the first ceramic layers (explained in the first embodiment, column 3, line 59-64); and a surface-mount IC device (130) mounted to a first surface of the substrate defined by one of the first ceramic layers, wherein said first and second regions are arranged for serial thermal interconnection between said IC device and an opposed heat sink (24). Polinski, though discloses the second region (148) with higher thermally conductivity (column 5, line 58-59), does not explicitly disclose thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive materials, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive materials of the first and second ceramic layers. However, Polinski further recites that additives can be added to improve the thermal conductivity (column 4, line 36-44).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the second region (148) be formed with thermally-conductive particles dispersed in a matrix comprising electrically-nonconductive materials, the thermally-conductive particles having a higher coefficient of thermal conductivity than the electrically-nonconductive materials of the first and second ceramic layers, in order to have higher thermal conductivity of the second region for fast dissipation of heat from the system.

Regarding claim 2, Polinski further discloses the substrate is a low-temperature co-fired ceramic substrate (sheets 122 and 148 made of low-temperature co-fired ceramic material, column 6, lien 1,2 and column 5, line 45).

Regarding claim 3, Polinski further discloses the thermally conductive particles are metal and/or ceramic particles (column 4, line 37-52).

Regarding claim 4, the substrate of Polinski does not have thermal via extending through the substrate from the surface mount device on the first surface to an oppositely disposed second surface of the substrate (no via in the second region 148, see figure).

Regarding claim 6, Polinski discloses all the features of the claimed invention but does not disclose the second ceramic layers have a coefficient of thermal expansion

of within about 4 ppm/°C of first ceramic layers. However, it is advisable to control the coefficient of thermal expansion of both layers of first and second region to avoid developing cracks at the bonding junction due the uneven expansion. Further the coefficient of thermal expansion will depend upon the additive used in the layers and can be controlled by changing the proportion and type of additives. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to keep the coefficient of thermal expansion as close as possible to that of the first ceramic layers, and for that matter within about 4 ppm/°C of first ceramic layers, in order to avoid crack development at the bonding junction.

Regarding claim 7, Polinski discloses all the features of the claimed invention including the second ceramic layers but does not disclose the second ceramic layers have a thermal conductivity of at least 10 W/mK. However, as applied to claim 1 above, additives are added to improve the thermal conductivity to the desired value to facilitate faster heat removal to protect the device from the damage. Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide structure of Polinski with the second ceramic

layers have a thermal conductivity of at least 10 W/mK, in order to have desired thermal conductivity to avoid damage to the system due to higher temperature.

Regarding claim 8, Polinski discloses all the features of the claimed invention including the second region free of the first ceramic layers, the first ceramic layers are bonded surface-to-surface to form the first region of the substrate, and the first region is free of the second ceramic layers and is bonded to the second region of the substrate (see figure), but does not disclose the second ceramic layer is one of a plurality of second ceramic layers bonded surface-to-surface to form the second region of the substrate. However, the second region of Polinski is made of higher thermal conductivity to facilitate faster heat removal. Adding more layer will help in enhancing heat removal. Therefore, it would have been obvious to a person of ordinary skill in the art to modify the structure of Polinski having the second ceramic layer is one of a plurality of second ceramic layers bonded surface-to-surface to form the second region of the substrate, in order to enhance heat removal rate to avoid damage to the system.

Regarding claim 9, Polinski further discloses a heat sink (24) bonded to the substrate, the second region of the substrate being between the heat sink and the first region of the substrate (see figure).

Regarding claim 10, Polinski discloses all the features of the claimed invention including the first region and the second region and an a surface mount IC device

mounted to a first surface of the substrate and an opposed heat sink, as applied to claims 1, 4, 6, 7 and 8.

Response to Arguments

5. Applicant's arguments filed on April 4, 2006 have been fully considered but they are not persuasive. The applicant on page 14 of the response argues that the amended claim 1 specifies that thermal energy from the power chip 12 flows serially, first through upper (relative less thermally conductive) continuous region 32, and then through lower (relatively more thermally conductive) continuous region 34, and finally, to an opposed heat sink 20. Polinski neither disclose nor suggest such an arrangement. To the contrary, each of the Polinski embodiments discloses mounting the IC chip to the higher thermally conductive layer or heat sink.

This is not found persuasive. Polinski, in the embodiment of figure 5, disclose the IC chip (microelectronic component 130) mounted on the upper surface of the board, which are ceramic layers, with the heat sink (24) on the opposite side of the board. As a result the heat generated by the component will travel serially from the upper layer of the board to the heatsink (24) at the bottom of the board. Further regarding argument about the continuous region 32 and the continuous region 34, there are no such continuous regions recited in the claim.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sasaki (US Patent No. 5,998,043), in figure 4, discloses a device with a component (8) mounted on the ceramic substrate (1) on the upper surface and a heat sink (6) on the bottom with metallic layer (2, 3, 4) for better heat conduction from the component to the heat sink.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IP
June 24, 2006

IBPatel

ISHWAR PATEL
PRIMARY EXAMINER